Appl. No. 10/612,859
Examiner: Thao P Le, Art Unit 2818
In response to th Office Action dated May 12, 2004

Date: June 9, 2004
Attorney Docket No. 10112421

AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph at page 3, line 22 with the following rewritten paragraph.

Because the properties of the dielectric layer 18 are similar to those of the pad oxide layer 12, when etchant is used to dip pad oxide layer 12, the shallow trench isolation region 26 is inevitably etched so that the corner 22 of the ~~trench 20~~ trench 15 is exposed and an indentation 30 is formed adjacent to the corner 22 of the ~~trench 20~~ trench 15.

Please replace the paragraph at page 3, line 27 with the following rewritten paragraph.

Thus, when the gate oxide layer and gate conductive layer are formed later, the conductive layer deposited in the indentation 30 is not easily removed and a short circuit between the adjacent transistors easily occurs. In addition, since the gate oxide layer at the corner 22 of the the ~~trench 20~~ trench 15 is thinner than other places, a parasitic transistor is formed. When current goes through this parasitic transistor, as the curvature radius of the corner 22 of the ~~trench 20~~ trench 15 is small, the electric fields concentrate and the Fowler-Nordheim current increases, hence the insulating property of the gate oxide layer of the corner 22 degrades, resulting in abnormal element characteristics. For example, there may be a kink effect in I-V curvature of Id and Vg, which generates a double hump.

Please replace the paragraph at page 8, line 17 with the following rewritten paragraph.

Subsequently, a patterned photoresist (PR) layer (not shown in Fig. 4A) is coated on the surface of the second mask layer 106, and photolithography performed to define the photoresist pattern required. Moreover, the second mask layer 106, the first mask layer 104, and the pad insulating layer 102 are etched anisotropically (for example reactive ion etching), with the patterned photoresist acting as a mask.

Please replace the paragraph at page 9, line 22 with the following rewritten paragraph.

Subsequently, referring to FIG. 4D, anisotropic etching, for example RIE, is performed along the tapered profiles 108 of the second mask layer 106 to remove part of the second mask layer 106,

the first mask layer 104, the pad insulating layer 102 , and the semiconductor substrate 100 around the trenches 105. Then, the corners ~~110~~ of the trench 105 are chamfered, and a Y-shaped trench 105a is further formed. The depth 120a (for example, between 2700~3600Å) of the Y-shaped trench 105a is deeper than that of the original trench 105, and the aspect ratio of the Y-shaped trench is between 4~6.

Please replace the paragraph at page 10, line 13 with the following rewritten paragraph.

Subsequently, referring to FIG. 4G, a thermal oxidation process is performed to grow a shield layer 116 such as a liner oxide layer with a thickness of 50Å to 350Å in the bottom, sidewall, and chamfered corners of the trench 105a and the surface 117 of the ~~substrate 110~~ substrate 100.

Please replace the paragraph at page 10, line 18 with the following rewritten paragraph.

Subsequently, referring to FIG. 4H, an insulator layer 118, such as a silicon dioxide layer, with a thickness of 3000~5000Å is formed on the shield layer 116 by HDPCVD using ~~O2~~ O_2 and ~~SiH4~~ SiH_4 as reactants with Ar sputtering. Finally, referring to FIG. 4I, chemical mechanical polishing removes uneven insulator layer 118 to cover the shield layer 116 and leave the insulator layer 118 inside the trench 105a. The first mask layer 104 and the pad insulating layer 102 are then removed using adequate liquid or etching to expose the element region, as shown in FIG. 4J. Accordingly, the shallow trench isolation region 150 of the present invention is achieved. Preferably, the first mask layer 104 is removed by, for example, a hot phosphoric acid solution and the pad insulating layer 102 is removed by, for example, a HF solution.